IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Original): A demodulator circuit for emulating the down conversion of an input signal x(t) with a local oscillator (LO) signal, said demodulator circuit comprising:

a first mixer for receiving said input signal x(t), and mixing said input signal x(t) with a multi-tonal mixing signal φ1, to generate an output signal φ1 x(t);

a second mixer for receiving said signal φ1 x(t) as an input, and mixing said signal φ1 x(t) with a mono-tonal mixing signal φ2, to generate an output signal φ1 φ2 x(t);

a first signal generator for generating said multi-tonal mixing signal φ1;

a second signal generator for generating said mono-tonal mixing signal φ2, where φ1 * φ2 has significant power at the frequency of said local oscillator signal being emulated; and

a power measurement circuit for measuring the power of said output signal φ1 φ2 x(t);

said second signal generator receiving a power level signal output from said power measurement circuit, and varying the characteristics of said mono-tonal mixing signal φ2 to reduce the power level of said output signal φ1 φ2 x(t).

Claim 2 (Original): The circuit of claim 1 wherein said second signal generator varies the frequency of said φ2 signal.

Claim 3 (Original): The circuit of claim 2 wherein said second signal generator comprises a voltage controlled oscillator (VCO).

Claim 4 (Original): The circuit of claim 3 wherein said second signal generator comprises:

a means for detecting changes in output power over time; and

a frequency control circuit which directs said VCO to incrementally adjust the frequency of said φ2 signal in response to changes in output power over time.

Claim 5 (Original): The circuit of claim 4 wherein said frequency control circuit responds to a failing trend in said power level over time by directing said VCO to continue adjusting the frequency of said φ2 signal in the same manner that it has been.

Claim 6 (Original): The circuit of claim 4 wherein said frequency control circuit responds to a rising trend in said power level over time by directing said VCO to invert the sense of the incremental adjustments being made to the frequency of said φ2 signal.

Claim 7 (Original): The circuit of claim 4 wherein said frequency control circuit further comprises means for smoothing changes in values of said output power, improving stability.

Claim 8 (Original): The circuit of claim 4 wherein said means for detecting changes in output power comprises:

a power measurement device with digital output;

a time delay device for receiving said digital output from said power measurement device and delaying said digital output; and

a comparator for comparing a current digital output to a delayed digital output, thereby determining whether power level is rising or falling over time.

Claim 9 (Original): The circuit of claim 5 further comprising a means for setting initial conditions of said frequency control circuit.

Claim 10 (Original): The circuit of claim 5 further comprising a clock which establishes timing for sampling and processing of output power signals for said frequency control circuit.

Claim 11 (Original): The circuit of claim 2 wherein neither of said $\varphi 1$ nor said $\varphi 2$ signals have significant power at the carrier frequency of said input signal $x(t)$.

Claim 12 (Original): The circuit of claim 11 wherein neither of said $\varphi 1$ nor said $\varphi 2$ signals have significant power at the carrier frequency of said LO signal being emulated.

Claim 13 (Original): The circuit of claim 1 wherein said first signal generator comprises a signal generator for generating square wave signals.

Claim 14 (Original): The circuit of claim 1 wherein said second signal generator comprises a signal generator for generating square wave signals.

Claim 15 (Original): The circuit of claim 1 wherein unwanted power at baseband is minimized by adjusting the frequency of said $\varphi 2$ signal such that unwanted RF tones do not fall within the frequency range of the desired signal at baseband.

Claim 16 (Original): The circuit of claim 1 wherein unwanted power at baseband is minimized by adjusting the frequency of said φ2 signal so that the probability of unwanted RF tones falling within the frequency range of φ1 * φ2 x(t) is significantly reduced.

Claim 17 (Original): The circuit of claim 1 wherein said second signal generator varies the phase of said φ2 signal.

Claim 18 (Original): The circuit of claim 1 wherein said second signal generator is responsive to noise in said output signal φ1 φ2 x(t) by adjusting the frequency of φ2.

Claim 19 (Original): The circuit of claim 3 wherein said first mixer comprises an active mixer.

Claim 20 (Original): The circuit of claim 19 wherein said first mixer comprises an active mixer having adjustable performance.

Claim 21 (Original): The circuit of claim 19 further comprising a high pass filter electrically connected between said first mixer and said second mixer.

Claim 22 (Original): The circuit of claim 21 wherein said second mixer comprises a passive mixer.

Claim 23 (Original): The circuit of claim 22, wherein each of said active mixer, said high pass filter and said passive mixer is a differential device.

Claim 24 (Original): A method of emulating the demodulation of an input signal x(t) to the product of said input signal with a local oscillator (LO) signal, said method comprising the steps of:

generating a multi-tonal mixing signal φ1;

generating a mono-tonal mixing signal φ2, where φ1 * φ2 has significant power at the frequency of the local oscillator signal being emulated, and neither of said φ1 nor said φ2 having significant power at the frequency of said input signal x(t), said LO signal being emulated, or an output signal φ1 φ2 x(t);

mixing said input signal x(t) with said multi-tonal mixing signal φ1, to generate an output signal φ1 x(t);

mixing said signal φ1 x(t) with said mono-tonal mixing signal φ2, to generate said output signal φ1 φ2 x(t);

measuring the power of said output signal φ1 φ2 x(t); and

adjusting the characteristics of said mono-tonal mixing signal φ2 to minimize the power of said output signal φ1 φ2 x(t).

Claim 25 (Original): A computer readable memory medium for storing software code executable to perform the method steps of claim 24.

Claim 26 (Canceled).